
Chapter 4 — Network Clocking

Overview

Need for synchronization

When digital signals are being transported over a communication link, the receiving end must operate at the same frequency (data rate) as the originating end to prevent loss of information. This is referred to as link synchronization. If both ends of a communication link are not in synchronization, data bit slips occur and therefore a loss of data results. In general, accurate timing is very important, but more importantly synchronized timing is a must for reliable data transfer.

When only two Meridian 1 switches are interconnected, synchronization can be achieved by operating the two systems in a master/slave mode whereby one system derives its timing from the other. However, in a network of digital systems, slips can be better prevented by forcing all digital systems to use a common reference clock (see Figure 68).

Synchronization methods

There are two common methods of maintaining timing coordination between switching systems.

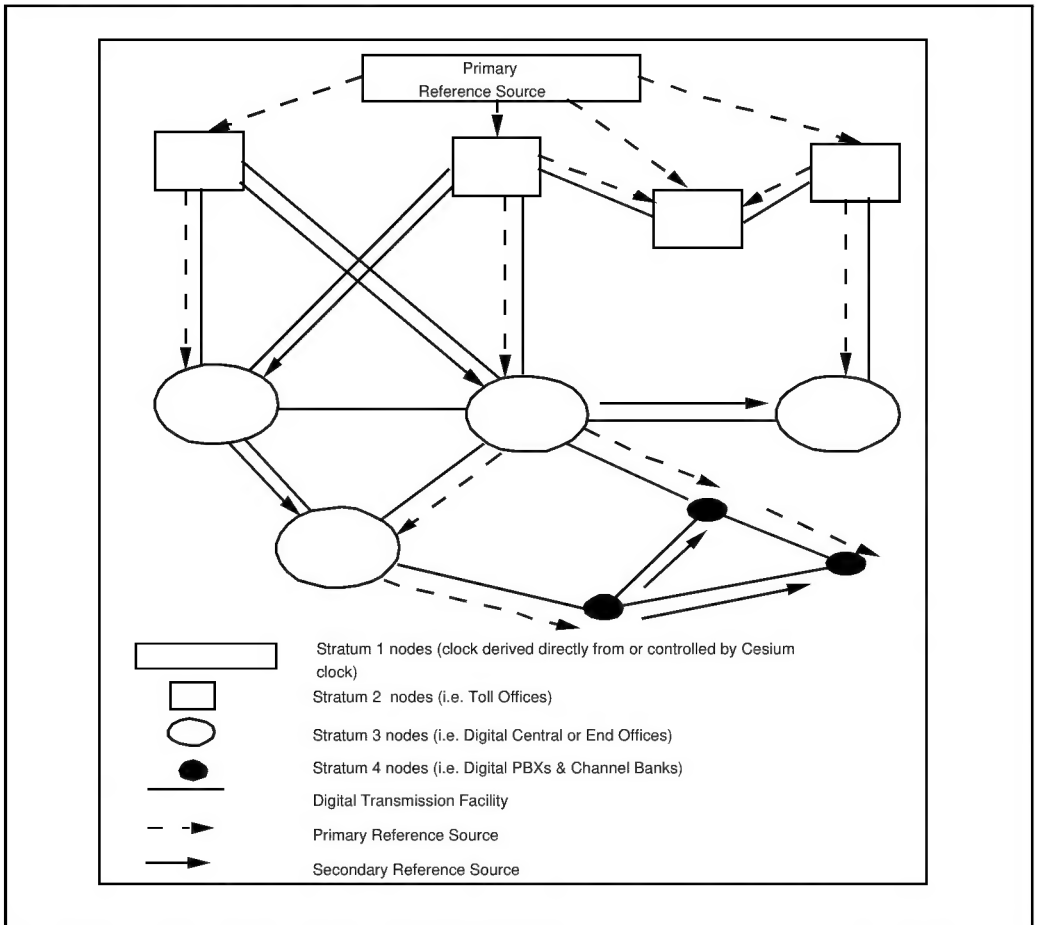
- a **Plesiosynchronous operation:** nodal clocks run independently (free run) at the same nominal frequency. There are frequency differences between clocks resulting in frame slips (see section “Frame Slips”). The magnitude of frame slips are directly proportional to the frequency difference. Slips are inevitable but can be minimized by using very stable clocks and elastic stores or buffers. These buffers are capable of absorbing a certain number of data bits to compensate for slight variances in clock frequencies.
- b **Mesosynchronous operation:** nodal clocks are continuously and automatically locked to an external reference clock. With this method, frame slips can be eliminated if elastic stores are large enough to compensate for transmission variances. Mesosynchronous operation is virtually slip free.

Whenever possible the Meridian 1 PBX uses the Mesosynchronous mode of operation by using the Clock Controller circuit cards to lock onto an external reference source (i.e. the Central Office, another Meridian 1 PBX, etc.). The above statement is true unless the Meridian 1 is used as a Master in an independent/private network (no digital links to a higher Node Category).

Hierarchical synchronization

Figure 68 provides a general view of a Digital Network Synchronization including the four stratum levels Node Categories of clocks (Stratum 1 being the highest--most accurate to Stratum 4 being the lowest). Meridian 1 clocking meets Node Category E--Stratum 4 requirements. Also shown are ways of providing a Secondary Clock Source while preventing timing loops.

Figure 68
Hierarchical Synchronization



Stratum Levels

In a digital network, nodes are synchronized using a priority master/slave method. Digital nodes are ranked in Stratum levels 1 to 5. Each node is synchronized to the highest ranking node in its neighborhood with which it has a direct link.

	Stratum 2	Stratum 3	Stratum 4
Accuracy	$\pm 1.6 \times 10^{-8}$ Hz	$\pm 4.6 \times 10^{-6}$ Hz	$\pm 3.2 \times 10^{-5}$ Hz
Holdover	1×10^{-10} per day	≤ 255 frame slips in 1st 24 hours	Not Required
Hardware Duplication	Required	Required (Note 1)	Not Required
MTIE During Rearrangement	MTIE ≤ 1 msec Phase Change Slope: ≤ 81 ns in any 1.326 msec	MTIE ≤ 1 msec Phase Change Slope: ≤ 81 ns in any 1.326 msec	No Requirement (Note 2)
Pull-in Range	3.2×10^{-8} Hz	9.2×10^{-6} Hz	6.4×10^{-5} Hz
Dedicated Timing Required	Required	Required	Not required

Note 1: Non-duplicated clock hardware that meets all other stratum 3 requirements is referred to as stratum 3ND.

Note 2: Stratum 4 clock hardware that meets MTIE requirements during rearrangements is referred to as 4E.

Frame Slip

Digital signals must have accurate clock synchronization for data to be interleaved into or extracted from the appropriate timeslot during multiplexing and demultiplexing operations. A Frame Slip is defined (for 2 Mb links) as the repetition of, or deletion of the 256 data bits of a CEPT frame due to a sufficiently large discrepancy in the read and write rates at the buffer (clocks aren't operating at exactly the same speed).

When data bits are written into (added to) a buffer at a slightly *higher* rate than that at which they are being read (emptied), sooner or later the buffer overflows. This is a slip-frame deletion.

In the opposite situation, when data bits are written (added) into a buffer at slightly *lower* rate than that at which they are being read (emptied), eventually the buffer runs dry or underflows. This is also a slip-frame repetition.

A 2 Mb PRI contains a buffer large enough to contain 2 full frames ($256 \times 2 = 512$ bits), and is normally kept half full (1 frame). See the following table for the impact of one slip on various types of data.

All of the degradations shown in the following table can be controlled or avoided by proper clock (network) synchronization.

Performance Impact of one Slip.

Service	Potential Impact
Encrypted Text	Encryption key must be resent.
Video	Freeze frame for several seconds. Loud pop on audio.
Digital Data	Deletion or repetition of Data. Possible Misframe.
Facsimile	Deletion of 4-8 scan lines. Drop Call.
Voice Band Data	Transmission Errors for 0.01 to 2 s. Drop Call.
Voice	Possible Click

Guidelines

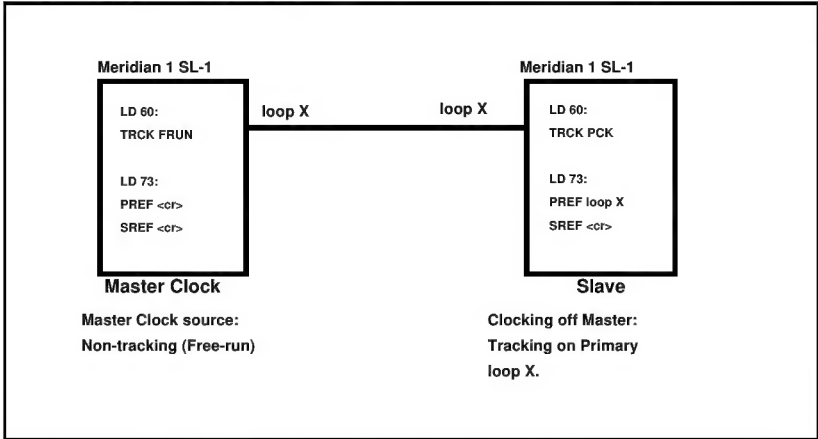
Some key points to keep in mind when designing Network Synchronization:

- Where possible, the Master Clock Source should always be from a Node Category/Stratum with higher clock accuracy—i.e. PBX connected to the C.O.; the CO is the Master and the PBX is the Slave.
- The source should not be in free-run itself (providing its own clock) unless it is operating in a fully independent network where the source acts as a Master (see Plesiosynchronous operation).
- When connecting two PBXs together (no CO connections), the most reliable PBX should be the Master. Reliability here refers to Dual CPU/Dual Clock, battery back-up or stratum level of the clock controller.

- Avoid timing loops. A timing loop occurs when a clock using as its reference frequency a signal that it itself traceable to the output of that clock. The formation of such a closed timing loop leads to frequency instability and is not permitted. Timing loops are sometimes unavoidable on the secondary clock reference source.
- Ensure all CO/PBX links used as clock references have a traceable path back to the same stratum 1 clock source.

While it is beyond the scope of this guide to provide detailed Network Synchronization, the following examples illustrate some of the basic concepts to achieve stable clocking.

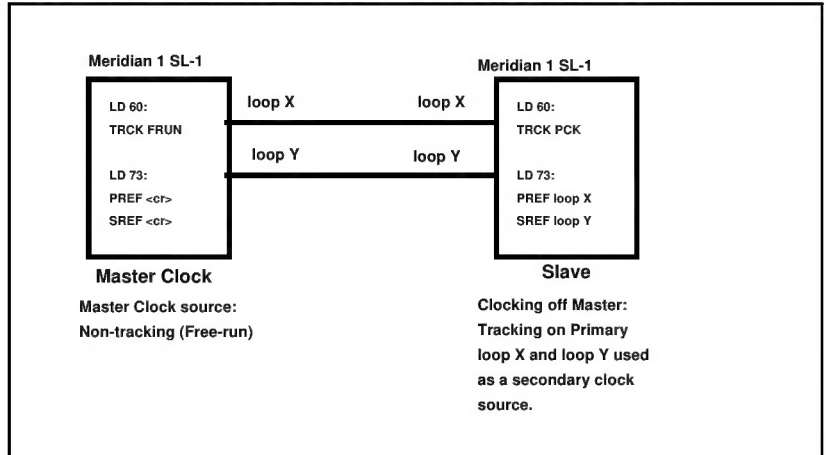
Example 1
Isolated Private Network



In this example, there is no digital connection to the Central Office.

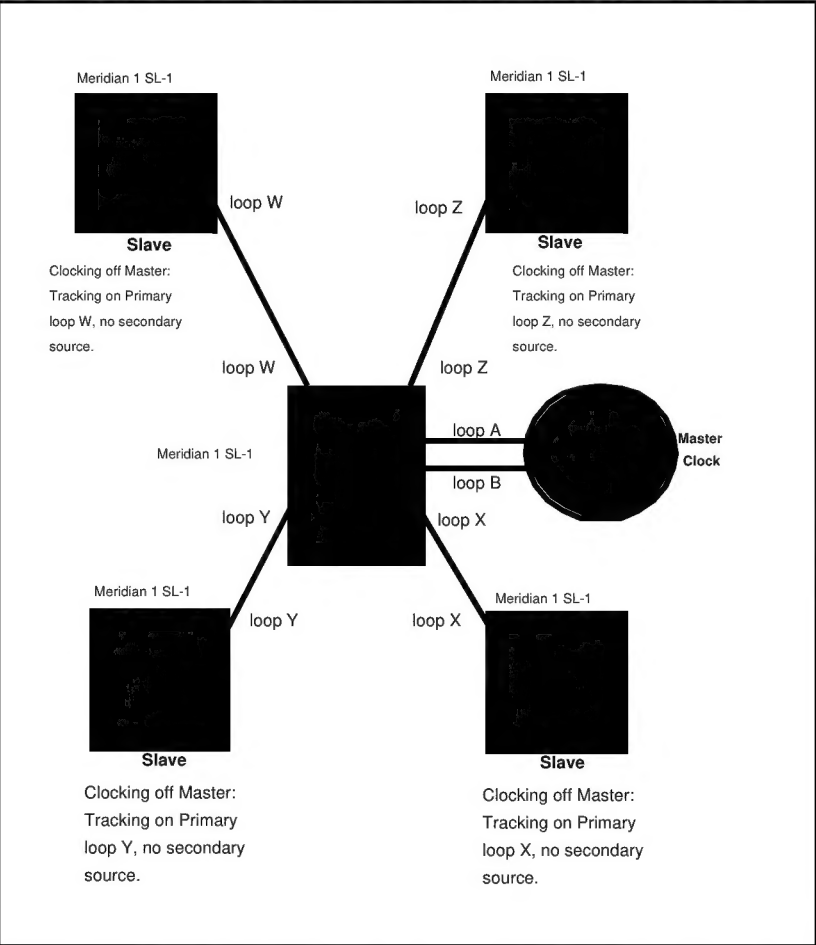
Example 2

Isolated Private Network with Secondary Reference Clock



In this example, there is no digital connection to the Central Office. For tie lines between PBXs facilitated by a central office, clocking is derived from the PBX, not the CO. When a second Digital loop is available, it can be used as a Secondary Clock source in case the Primary Source fails.

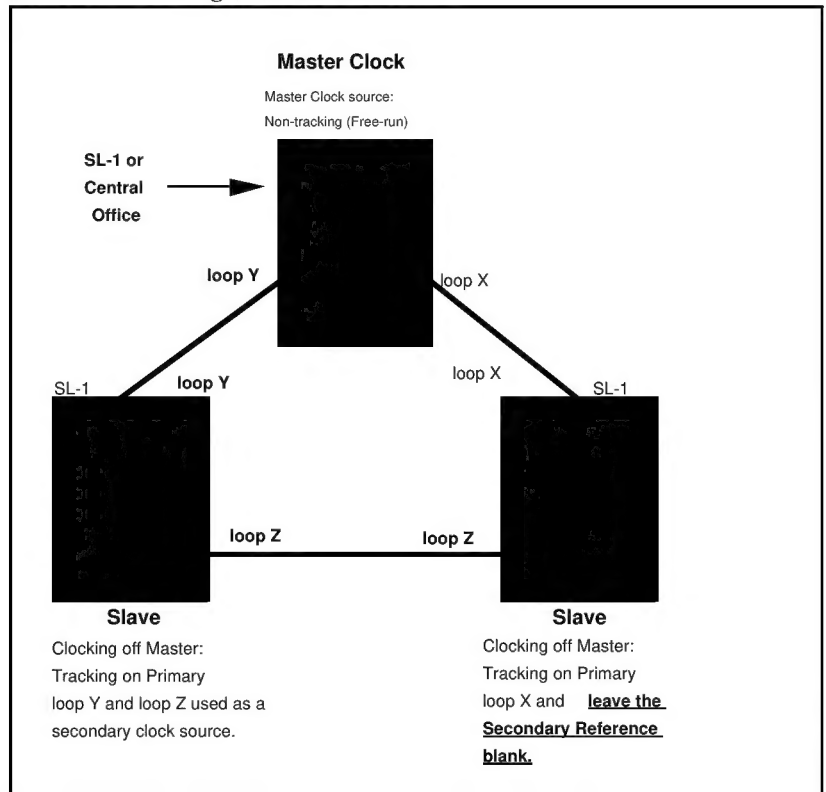
Example 3
Clocking Hierarchy referenced to a Public Network Master Clock



This is an example of a “STAR” arrangement— one Hub PBX is linked to the Central Office and all other PBXs are connected as slaves. When a second Digital loop from the Meridian 1 which forms the hub of this network becomes available, it can be used as a Secondary Clock Source in case the Primary Source fails.

Example 4

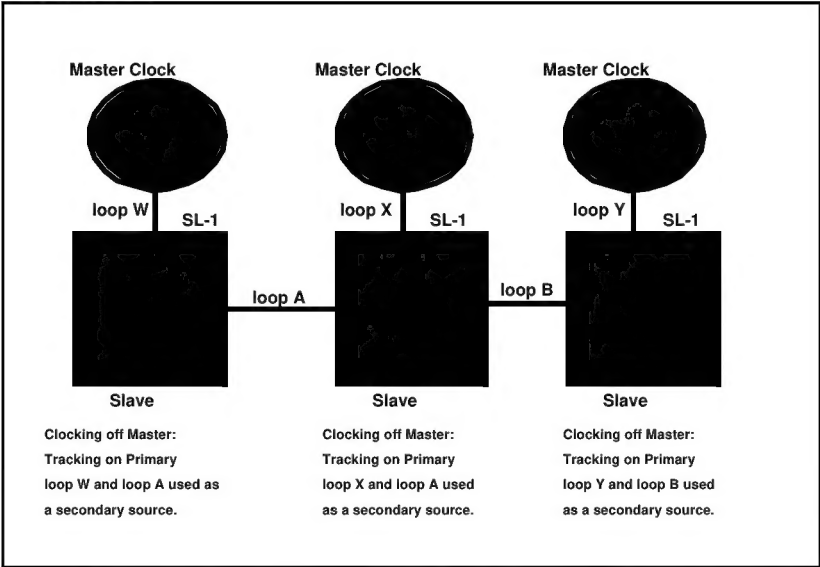
Alternate Clocking from the same CO



In this case, a digital connection to the Central Office may exist (i.e. Loops X and Y). When a second Digital loop from the CO or Master M-1 becomes available, it can be used as a Secondary Clock Source in case the Primary Source fails.

To avoid timing loops, in example 4-4 the most reliable slave system should not have a Secondary Clock Source (SREF= <cr>). In this example, this is illustrated by the node which supports loops X and Z.

Example 5

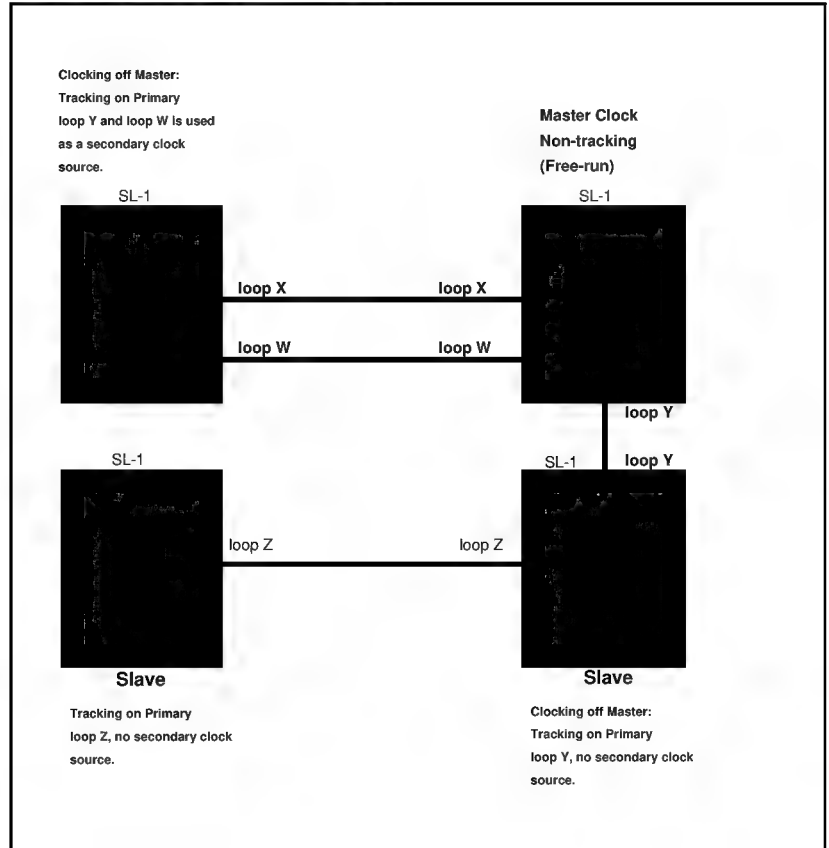


Here, digital connections to the Central Office do exist. When a second Digital loop from the CO becomes available, it can be used as a Secondary Clock Source in case the Primary Source fails.

Slaves can track on each other as a secondary source since the chances of both links to the Central Offices going down at the same time are minimal (very unlikely).

All central offices must have a path back to the same stratum 1 source.

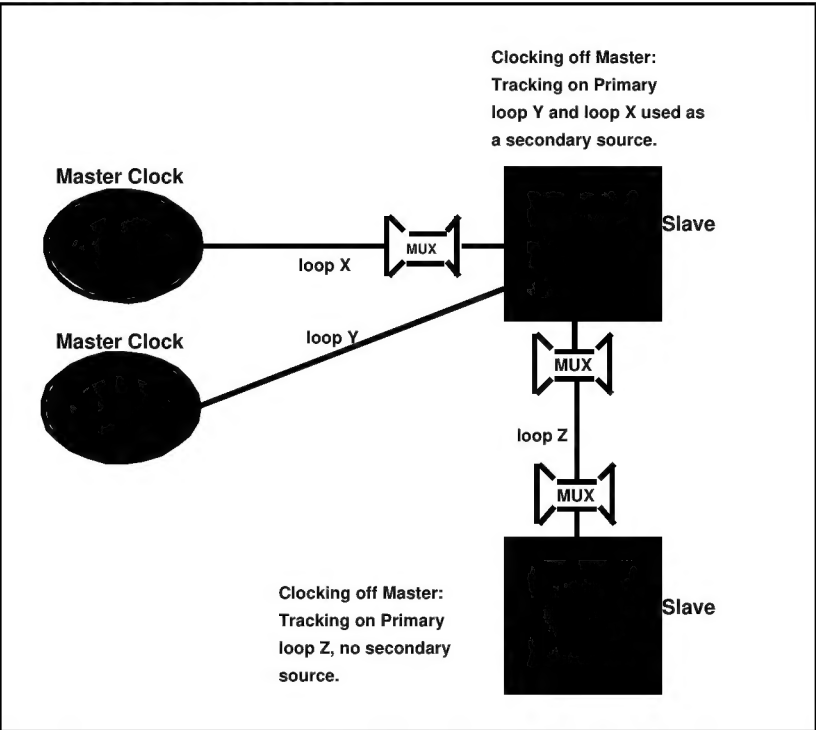
Example 6 Complex Isolated Private Network



Digital connections to the Central Office do not exist in this example. If it does, the PBX connected to it will track off the CO and will in turn be used as a clock source to other nodes.

When a second Digital loop from the Master Meridian 1/SL-1 becomes available, it can be used as a Secondary Clock Source in case the Primary Source fails.

Example 7
Network Clocking with MUX



The direct connection to the CO (without a MUX) should be used as a primary clock reference since there is the least amount of hardware involved. The MUX must pass the clock and not generate its own clock; in other words, it must also be a slave (not Free Run). Synchronized clocking is required.

Digital Trunks

Synchronization, Option 11

Digital trunk synchronization is provided via a Clock Controller on the digital trunk pack.

There are two modes of operation:

Tracking Mode

In tracking mode, the Primary Rate Interface (PRI) or Digital Trunk Interface (DTI) loop supplies an external clock reference to the on-board clock controller. Two PRI or DTI packs can operate in tracking mode, with one defined as the primary reference source for clock synchronization, the other defined as a secondary reference source. The secondary reference acts as a back-up to the primary reference.

Free Run (Non-Tracking Mode)

The clock synchronization for a PRI loop may operate in free-run mode if:

- the loop is not defined as the primary or secondary clock reference
- the primary and secondary references are disabled
- the primary and secondary references are in a local alarm state

For Option 11 systems, a single cable supports either PRI or DTI;

PRI/DTI — LTU 20 ft NTB05CA

Option 11 clock controllers

Digital trunking requires synchronized clocking so that a shift in one clock source will result in an equivalent shift of the same size and direction in all parts of the network.

The Option 11 system supports a single clock controller (CC) located on either:

- the NTAK10 2 Mb DTI
- the NTAK79 2 Mb PRI
- the NTBK50 2 Mb PRI
- the NTBK22 MISP (BRI applications).

This clock controller can operate in one of two modes: tracking, or non-tracking (also known as free-run).

The Clock Controller circuitry synchronizes the Option 11 to an external reference clock and generates and distributes the clock to the system. This enables the Option 11 to function either as a slave to an external clock or as a clocking master.

Note: When configuring ISL over analogue trunks, clock controllers are not required.

Tracking mode

In tracking mode, a reference clock is supplied to the clock controller. The clock controller uses this reference to adjust the system clock so that the two are of the same frequency. The CC is capable of tracking to a primary or secondary reference supplied on the DTI/PRI/BRI circuit card, or to an external reference clock.

When tracking using a reference clock derived from a DTI/PRI/BRI source, an optional secondary clock source can be defined. The primary clock source is derived from the clock controller's host circuit card. The secondary source may be defined as any other DTI/PRI/BRI installed in the Option 11 system. The secondary reference acts as a back-up to the primary reference.

There are two stages to clock controller tracking:

- tracking a reference, and
- locked onto a reference.

When tracking a reference, the clock controller uses an algorithm to match its frequency to the frequency of the incoming clock. When the frequencies are very near to being matched, the clock controller is locked onto the reference. The clock controller will make small adjustments to its own frequency until both the incoming and system frequencies correspond.

If the incoming clock reference is stable, the internal clock controller tracks it, locks onto it, and matches frequencies exactly. Occasionally, however, environmental circumstances cause the external or internal clocks to drift. When this happens, the internal clock controller briefly enters the tracking stage.

If the incoming reference is unstable, the internal clock controller is continuously in the tracking stage. This condition does not present a problem, rather, it shows that the clock controller is continually attempting to lock onto the signal. If slips are occurring, however, it means that there is a problem with the clock controller or the incoming line.

Free-run (non-tracking)

In Free-Run (Non-tracking) mode, the clock controller does not synchronize on any source, it provides its own internal clock to the system. This mode can be used when the Option 11 is used as a master clock source for other systems in the network. Free-run mode is undesirable if the Option 11 is intended to be a slave. It can occur, however, when both the primary and secondary clock sources are lost due to hardware faults. It can also be turned on manually using software commands.